PATENT
Docket No. 0023-0003

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	)	
	)	
Ross Suydam HEITKAMP	)	
	)	
Serial No.: 09/749,585	)	Group Art Unit: 2112
	)	
Filed: December 28, 2000	)	Examiner: K. Huynh
	)	
For: SYSTEMS AND METHODS FOR RELIABLY SELECTING BUS MASTERSHIP IN A FAULT TOLERANT MANNER	)	

U.S. Patent and Trademark Office
Customer Window, Mail Stop Appeal Brief - Patents
Randolph Building
401 Dulany Street
Alexandria, VA 22314

APPEAL BRIEF

This Appeal Brief is submitted in response to the final Office Action, dated February 9, 2005, and in support of the Notice of Appeal, filed May 4, 2005.

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is Juniper Networks, Inc.

II. RELATED APPEALS, INTERFERENCES, AND JUDICIAL PROCEEDINGS

Appellant is unaware of any related appeals, interferences or judicial proceedings.

III. STATUS OF CLAIMS

Claims 1-28 are pending in this application.

Claims 9-16 and 28 have been finally rejected under 35 U.S.C. § 102(e) as anticipated by Cranston et al. (U.S. Patent No. 6,253,269).

Claims 1, 2, 5-8, 17, 18, 20, 21, 23, and 25-27 have been finally rejected under 35 U.S.C. § 103(a) as unpatentable over Jaramillo et al. (U.S. Patent No. 6,598,104) in view of Wang et al. (US 2004/0098525).

Claims 3, 19, and 24 have been finally rejected under 35 U.S.C. § 103(a) as unpatentable over Jaramillo et al. in view of Wang et al. and Nakamura (U.S. Patent No. 6,622,191).

Claims 4 and 22 have been finally rejected under 35 U.S.C. § 103(a) as unpatentable over Jaramillo et al. in view of Wang et al. and Melo et al. (U.S. Patent No. 5,553,248).

Claims 1-28 are the subject of the present appeal. These claims are reproduced in the Claim Appendix of this Appeal Brief.

IV. STATUS OF AMENDMENTS

No amendments have been filed subsequent to the final Office Action, dated February 9, 2005.

V. SUMMARY OF CLAIMED SUBJECT MATTER

In the paragraphs that follow, each of the independent claims and the claims reciting means-plus-function or step-plus-function language that is involved in this appeal will be recited followed in parenthesis by examples of where support can be found in the specification and

drawings.

Claim 1 recites a system for selecting bus mastership in a multi-master system (100), comprising: a plurality of master devices (110, 120) configured to generate control signals (160-190) relating to control of a bus (140, 150) in the multi-master system (100) (page 11, lines 10-13); and a plurality of slave devices (130) connected to the master devices (110, 120) via the bus (140, 150, 610), each of the slave devices being configured to: receive the control signals (160-190) from the master devices (110, 120) (page 11, lines 13-14), determine whether a conflict in the control signals (160-190) exists (page 11, line 14 - page 12, line 4), generate one or more alternate control signals (250, 260) for selecting bus mastership when a conflict is determined to exist (page 12, lines 5-14), and determine which of the master devices (110, 120) obtains control of the bus (140, 150, 610) using the one or more alternate control signals (250, 260) when a conflict is determined to exist (page 12, lines 15-16; page 5, lines 11-14).

Claim 8 recites a system for selecting a master in a multi-master system (100), comprising: means for outputting first and second control signals (160-190) relating to mastership in the multi-master system from each of a plurality of masters (110, 120) in the multi-master system (100) (page 11, lines 10-13); means for determining whether a conflict for mastership exists based on the first and second control signals (160-190) (page 11, line 13 - page 12, line 4); means for generating a switch signal (250) and a select signal (260) when a conflict is determined to exist (page 12, lines 5-14); and means for selecting one of the masters (110, 120) using the switch signal (250) and the select signal (260) (page 12, lines 15-16; page 5, lines 11-14).

Claim 9 recites a method for selecting a bus (140, 150) in a multi-bus system (100),

comprising: generating control signals (160-190) relating to bus selection in the multi-bus system (100) (page 10, lines 13); determining whether a conflict for bus selection exists based on the control signals (160-190) (page 11, line 13 - page 12, line 4); generating one or more alternate control signals (250, 260) when a conflict is determined to exist (page 12, lines 5-14); and selecting a bus (140, 150) using the one or more alternate control signals (250, 260) (page 12, line 15-16).

Claim 17 recites a computer-readable medium that stores instructions executable by one or more processors to perform a method for selecting a master in a multi-master system (100), comprising: instructions for outputting a plurality of control signals (160-190) relating to selection of a master from each of a plurality of masters (110, 120) in the multi-master system (100) (page 11, lines 10-13); instructions for determining whether a conflict for selection of a master exists based on the control signals (160-190) (page 11, line 13 - page 12, line 4); instructions for generating a switch control signal (250) and a select control signal (260) when a conflict is determined to exist (page 12, line 5-14); and instructions for selecting one of the masters (110, 120) using the switch control signal (250) and the select control signal (260) (page 12, lines 15-16).

Claim 18 recites in a multi-master system (100) comprising a plurality of master devices (110, 120) connected to a plurality of slave devices (130), each of the slave devices (130) comprising: selection logic (210) configured to determine whether control signals (160-190) from the master devices (110, 120) indicate that two or more of the master devices (110, 120) concurrently assert mastership within the multi-master system (100) (page 7, lines 7-14), generate a conflict indication signal (240) when two or more of the master devices (110, 120)

concurrently assert mastership (page 7, lines 7-14), and select mastership using one or more alternate control signals (250, 260) when two or more of the master devices (110, 120) concurrently assert mastership (page 8, lines 4-5); and conflict resolution logic (220) configured to generate the one or more alternate control signals (250, 260) to identify mastership in response to the conflict indication signal (240) (page 7, line 21 - page 8, line 4).

Claim 23 recites a method for selecting bus mastership in a multi-master system (100) comprising a plurality of master devices (110, 120) connected to a plurality of slave devices (130) via at least one bus (140, 150), the method, performed by each of the slave devices (130), comprising: determining whether control signals (160-190) from the master devices (110, 120) indicate that two or more of the master devices concurrently assert bus mastership (page 11, line 13 - page 12, line 4); generating one or more alternate control signals (250, 260) to identify which of the master devices (110, 120) obtains bus mastership when two or more of the master devices (110, 120) concurrently assert bus mastership (page 12, lines 5-14); determining which of the master devices (110, 120) obtains bus mastership using the one or more alternate control signals (250, 260) when two or more of the master devices (110, 120) concurrently assert bus mastership (page 12, lines 15-16); and determining which of the master devices (110, 120) obtains bus mastership using the control signals (160-190) when one of the master devices (110, 120) asserts bus mastership (page 9, lines 5-12).

Claim 27 recites a multi-master system (500), comprising: a plurality of master devices (110, 120) configured to generate control signals (160-190) relating to bus mastership (page 5, line 16 - page 6, line 3); conflict resolution logic (510) configured to receive the control signals from the master devices (110, 120) (page 13, lines 7-8), determine whether the control signals

(160-190) indicate that two or more of the master devices (110, 120) concurrently assert bus mastership (page 13, lines 7-8), and generate a switch signal (520) and a select signal (530) when it is determined that two or more of the master devices (110, 120) concurrently assert bus mastership (page 13, lines 8-15); and a plurality of slave devices (130) configured to select bus mastership using the switch signal (520) and the select signal (530) when the control signals (160-190) indicate that two or more of the master devices (110, 120) concurrently assert bus mastership (page 13, lines 15-17).

Claim 28 recites a multi-bus system (100), comprising: a plurality of buses (140, 150); a plurality of master devices (110, 120) corresponding to the buses (140, 150), each of the master devices (110, 120) controlling a corresponding one of the buses (140, 150), the master devices (110, 120) generating control signals (160-190) that indicate which of the buses (140, 150) is an active bus (page 11, lines 10-13); and a plurality of slave devices (130) connected to each of the buses (140, 150) and configured to receive the control signals (160-190) (page 11, lines 13-14), determine whether the control signals (160-190) indicate that two or more of the buses (140, 150) are declared active buses (page 11, line 14 - page 12, line 4), generate alternate control signals (250, 260) when the control signals (160-190) indicate that two or more of the buses (140, 150) are declared active buses (page 12, lines 5-14), and select one of the buses (140, 150) as the active bus using the alternate control signals (250, 260) (page 12, lines 15-16).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Claims 9-16 and 28 stand rejected under 35 U.S.C. § 102(e) as anticipated by Cranston et al.

B. Claims 1, 2, 5-8, 17, 18, 20, 21, 23, and 25-27 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Jaramillo et al. in view of Wang et al.

C. Claims 3, 19, and 24 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Jaramillo et al. in view of Wang et al. and Nakamura.

D. Claims 4 and 22 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Jaramillo et al. in view of Wang et al. and Melo et al.

VII. ARGUMENT

A. Rejection Under 35 U.S.C. § 102(e) Over Cranston et al. (U.S. Patent No. 6,253,269).

1. Claims 9 and 14.

The initial burden of establishing a prima facie basis to deny patentability to a claimed invention is always upon the Examiner. In re Oetiker, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). For a proper rejection under 35 U.S.C. § 102, each and every element as set forth in the claim must be found, either expressly or inherently, in a single prior art reference. Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 2 USPQ2d 1051 (Fed. Cir. 1987). Prior legal precedent requires that the identical invention be shown in as complete detail as is contained in the claim. Richardson v. Suzuki Motor Co., 868 F.2d 1226, 9 USPQ2d 1913 (Fed. Cir. 1989).

With these principles in mind, Appellant submits that independent claim 9 is patentable over Cranston et al. Independent claim 9 is directed to a method for selecting a bus in a multi-bus system. The method comprises generating control signals relating to bus selection in the multi-bus system; determining whether a conflict for bus selection exists based on the control

signals; generating one or more alternate control signals when a conflict is determined to exist; and selecting a bus using the one or more alternate control signals.

Cranston et al. does not disclose or suggest the combination of features recited in claim 9. For example, Cranston et al. does not disclose or suggest generating one or more alternate control signals when a conflict for bus selection is determined to exist. The Examiner alleged that Cranston et al. discloses this feature and cited column 7, lines 17-37, and column 4, lines 1-22, of Cranston et al. for support. Final Office Action, page 2. Appellant respectfully disagrees.

At column 7, lines 17-37, Cranston et al. discloses:

> It should be understood that the arbiter 50 can use a variety of procedures to select between the plurality of communication buses. FIG. 10 shows a general method that can be utilized by the arbiter 50 to select the appropriate communication bus to interface to the application card 20. At Step 100, the arbiter 50 monitors the plurality of communication buses to determine if a communication buses has become active with data from a management card. At Step 102, an active communication bus can be determined in any variety of ways well known to those skilled in the art including monitoring protocols sent on the communication buses.
>
> At Step 104, the active communication bus is allowed access to the application card by connecting or switching the active communication bus to the local bus of the application card. The access to the local card can be provided by a switching function device implemented through an integrated switching matrix, a simple decoder or other solid state integrated circuit. At Step 106, the arbiter prevents the other communication buses from accessing the application card to prevent possible conflicts and contention between the buses.

In this section, Cranston et al. discloses that the arbiter permits access to the application card to an active communication bus and prevents access to other communication buses. Nowhere in this section, or elsewhere, does Cranston et al. disclose generating one or more alternate control signals when a conflict for bus selection is determined to exist, as required by claim 9.

At column 4, lines 1-22, Cranston et al. discloses:

> . . . also possible to combine multiple master devices and multiple slave devices, onto an I^2C-bus to form a multi-master system. In this multi-master system, if more than one

> master device simultaneously attempts to control the line a conflict arises and an arbitration procedure must decide which master device gets priority.
>
> In addition to communication conflicts over a single bus, multiple I^2C-buses accessing the same application card may also potentially conflict. In some systems, several I^2C-buses may exist for redundancy and fault tolerant operation. As previously described, a card chassis holding a number of application cards may include a management card such as Switch Fabric/Management Card 26 to control the operation of the card chassis and application cards within the chassis. To provide for fault tolerant operation, a plurality of management cards may be provided for backup and redundancy. Each of the management cards will have its own communication bus access to each application card. These redundant management communication buses, however, should have mutually exclusive data communication access to the application card to avoid conflicts and contention between multiple devices.

In this section, Cranston et al. discloses that if more than one master device simultaneously attempts to control the line a conflict arises and an arbitration procedure must decide which master device gets priority. Cranston et al. does not disclose or suggest, however, that the arbitration procedure generates one or more alternate control signals when a conflict for bus selection is determined to exist, as would be required by claim 9.

Because Cranston et al. does not disclose or suggest generating one or more alternate control signals, Cranston et al. cannot disclose or suggest selecting a bus using the one or more alternate control signals, as further recited in claim 9. The Examiner alleged that Cranston et al. discloses this feature and cited column 7, lines 17-56, of Cranston et al. for support. Final Office Action, page 2. Appellant respectfully disagrees.

At column 7, lines 17-56, of which lines 17-37 have been reproduced above, Cranston et al. discloses:

> Because the I^2C-bus is bidirectional, the arbiter also preferably includes knowledge of the I^2C protocol to appropriately switch the bus direction as described above.
>
> Alternatively, the arbiter may select among a plurality of communication buses according to a programmed algorithm or other criteria. A priority can be assigned to communication buses and the priority of the communication bus used to selected the appropriate

> communication bus to allow access to the application card. A priority can also be utilized to allow a communication bus to preempt communication buses of lower priority. Communication buses may be assigned to classes in which certain classes are allowed simultaneous access to the application card and other classes of communication buses access the card mutually exclusively. The management card may download updated priority scheme to the arbiter over to the I^2C-bus. Using the arbiter, any arbitrary scheme for selecting among a plurality of communication buses may be implemented and tailored and modified according to the needs of the particular device.

In this section, Cranston et al. discloses that buses may be selected based on the priorities assigned to the buses. Nowhere in this section, or elsewhere, does Cranston et al. disclose generating one or more alternate control signals when a conflict for bus selection is determined to exist or selecting a bus using the one or more alternate control signals, as required by claim 9.

Accordingly, it is respectfully submitted that claim 9 is not anticipated by Cranston et al. under 35 U.S.C. § 102. Reversal of the rejection of claim 9 is respectfully requested.

2. Claim 10.

Dependent claim 10 recites determining whether the control signals indicate that two or more of the buses are to be selected concurrently, and generating a conflict indication signal when the control signals indicate that two or more of the buses are to be selected concurrently. Initially, claim 10 depends from claim 9 and is, therefore, not anticipated by Cranston et al. for at least the reasons that claim 9 is not anticipated.

Further, Cranston et al. does not disclose or suggest the combination of features recited in claim 10. For example, Cranston et al. does not disclose or suggest generating a conflict indication signal when the control signals indicate that two or more of the buses are to be selected concurrently.

The Examiner alleged that Cranston et al. discloses this feature and cited column 3, line 52 - column 4, line 22 and column 7, lines 7-37, of Cranston et al. for support. Final Office

Action, page 3. Appellant respectfully disagrees.

At column 3, line 52 - column 4, line 22, Cranston et al. discloses:

> The Inter-IC bus or I^2C-bus in this exemplary embodiment is generally designed to connect a number of integrated circuit ("ICs") devices. The I^2C-bus is a multi-master bus, meaning that a plurality of devices, such as ICs, can be connected to the bus, and each of the devices may act as the master of the bus by taking control of the bus to initiate a data transfer. According to the I^2C-bus standard, a device that transmits signals onto the I^2C-bus is the "transmitter." A device that controls signal transfers on the bus in addition to controlling the clock frequency of the bus is the "master." A device that receives signals from the bus is the receiver and a device that is controlled by the master is a "slave." The master device can transmit or receive signals to or from a slave device, respectively, or control signal transfers between two slave devices, where one slave device is the transmitter and the other slave device is the receiver. It is also possible to combine multiple master devices and multiple slave devices, onto an I^2C-bus to form a multi-master system. In this multi-master system, if more than one master device simultaneously attempts to control the line a conflict arises and an arbitration procedure must decide which master device gets priority.
>
> In addition to communication conflicts over a single bus, multiple I^2C-buses accessing the same application card may also potentially conflict. In some systems, several I^2C-buses may exist for redundancy and fault tolerant operation. As previously described, a card chassis holding a number of application cards may include a management card such as Switch Fabric/Management Card 26 to control the operation of the card chassis and application cards within the chassis. To provide for fault tolerant operation, a plurality of management cards may be provided for backup and redundancy. Each of the management cards will have its own communication bus access to each application card. These redundant management communication buses, however, should have mutually exclusive data communication access to the application card to avoid conflicts and contention between multiple devices.

In this section, Cranston et al. discloses that if more than one master device simultaneously attempts to control the line a conflict arises and an arbitration procedure must decide which master device gets priority. Nowhere in this section, or elsewhere, however, does Cranston et al. disclose or suggest that a conflict indication signal is generated when the control signals indicate that two or more buses are to be selected concurrently, as required by claim 10.

At column 7, lines 7-37, Cranston et al. discloses:

> An exemplary Read/Write State Machine 54 processes the reads and writes to and from the appropriate communication bus as determined from the Start/Stop Detection 52. FIGS.

> 9 and 10 show the illustrative flow charts of the Read/Write State Machine 54. It will be appreciated by those skilled in the art that the can implement the flow charts with a logic state machine using combinational logic. A stop condition on either communication bus resets the control state machine 56.
>
> It should be understood that the arbiter 50 can use a variety of procedures to select between the plurality of communication buses. FIG. 10 shows a general method that can be utilized by the arbiter 50 to select the appropriate communication bus to interface to the application card 20. At Step 100, the arbiter 50 monitors the plurality of communication buses to determine if a communication buses has become active with data from a management card. At Step 102, an active communication bus can be determined in any variety of ways well known to those skilled in the art including monitoring protocols sent on the communication buses.
>
> At Step 104, the active communication bus is allowed access to the application card by connecting or switching the active communication bus to the local bus of the application card. The access to the local card can be provided by a switching function device implemented through an integrated switching matrix, a simple decoder or other solid state integrated circuit. At Step 106, the arbiter prevents the other communication buses from accessing the application card to prevent possible conflicts and contention between the buses.

In this section, Cranston et al. discloses that the arbiter can use a variety of procedures to select between the plurality of communication buses and prevent other communication buses from accessing the application card to prevent possible conflicts and contention between the buses. Nowhere in this section, or elsewhere, however, does Cranston et al. disclose or suggest that the arbiter generates a conflict indication signal when the control signals indicate that two or more buses are to be selected concurrently, as required by claim 10.

Accordingly, it is respectfully submitted that claim 10 is not anticipated by Cranston et al. under 35 U.S.C. § 102. Reversal of the rejection of claim 10 is respectfully requested.

3. Claim 11.

Dependent claim 11 recites generating the one or more alternate control signals in response to the conflict indication signal. Initially, claim 11 depends from claims 9 and 10 and is, therefore, not anticipated by Cranston et al. for at least the reasons that claims 9 and 10 are not

anticipated.

Further, Cranston et al. does not disclose or suggest the combination of features recited in claim 11. For example, Cranston et al. does not disclose or suggest generating the one or more alternate control signals in response to the conflict indication signal that is generated when the control signals indicate that two or more of the buses are to be selected concurrently.

The Examiner alleged that Cranston et al. discloses this feature and cited column 3, line 52 - column 4, line 22 and column 7, lines 7-37, of Cranston et al. for support. Final Office Action, page 3. Appellant respectfully disagrees.

Column 3, line 52 - column 4, line 22 of Cranston et al. has been reproduced above. In this section, Cranston et al. discloses that if more than one master device simultaneously attempts to control the line, a conflict arises and an arbitration procedure must decide which master device gets priority. Nowhere in this section, or elsewhere, however, does Cranston et al. disclose or suggest generating one or more alternate control signals in response to a conflict indication signal that is generated when the control signals indicate that two or more of the buses are to be selected concurrently, as required by claim 11.

Column 7, lines 7-37, of Cranston et al. has been reproduced above. In this section, Cranston et al. discloses that the arbiter can use a variety of procedures to select between the plurality of communication buses and prevent other communication buses from accessing the application card to prevent possible conflicts and contention between the buses. Nowhere in this section, or elsewhere, however, does Cranston et al. disclose or suggest generating one or more alternate control signals in response to a conflict indication signal that is generated when the control signals indicate that two or more of the buses are to be selected concurrently, as required

by claim 11.

Accordingly, it is respectfully submitted that claim 11 is not anticipated by Cranston et al. under 35 U.S.C. § 102. Reversal of the rejection of claim 11 is respectfully requested.

4. Claim 12.

Dependent claim 12 recites that the one or more alternate control signals include a bus switch signal that indicates whether a change in bus selection is to occur and a bus select signal that indicates which of the buses is to be selected. Initially, claim 12 depends from claim 9 and is, therefore, not anticipated by Cranston et al. for at least the reasons that claim 9 is not anticipated.

Further, Cranston et al. does not disclose or suggest the combination of features recited in claim 12. For example, Cranston et al. does not disclose or suggest one or more alternate control signals that include a bus switch signal that indicates whether a change in bus selection is to occur and a bus select signal that indicates which of the buses is to be selected.

The Examiner alleged that Cranston et al. discloses these features and cited column 7, lines 7-37, and column 2, lines 18-32, of Cranston et al. for support. Final Office Action, page 3. Appellant respectfully disagrees.

Column 7, lines 7-37, of Cranston et al. has been reproduced above. In this section, Cranston et al. discloses that the arbiter can use a variety of procedures to select between the plurality of communication buses and prevent other communication buses from accessing the application card to prevent possible conflicts and contention between the buses. Nowhere in this section, or elsewhere, however, does Cranston et al. disclose or suggest one or more alternate control signals that include a bus switch signal that indicates whether a change in bus selection is

to occur and a bus select signal that indicates which of the buses is to be selected, as required by claim 12.

At column 2, lines 18-32, Cranston et al. discloses:

> According to another aspect of the present invention, the arbiter allows the application card to dynamically select or arbitrate between different communication buses. The arbiter may include state machine logic to implement appropriate protocol of the communication bus. The arbiter can employ a variety of different algorithms to allow and control access to the application card. The arbiter may allow access to the application card according to the priority of different communication buses. The arbiter can allow simultaneous access to the application card according to the types and classes of different communication buses. Using the present invention, any arbitrary scheme for selecting among a plurality of communication buses may be implemented and dynamically tailored and changed according to the needs of the particular device.

In this section, Cranston et al. discloses that the arbiter may allow access to an application card according to the priority of the different communication buses. Cranston et al. also indicates that any arbitrary scheme for selecting among a plurality of communication buses may be implemented. Cranston et al. does not disclose or suggest one or more alternate control signals that include a bus switch signal that indicates whether a change in bus selection is to occur and a bus select signal that indicates which of the buses is to be selected, as required by claim 12. The statement by Cranston et al. that any arbitrary scheme for selecting among a plurality of buses can be used is insufficient to suggest that Cranston et al. contemplated the use of one or more alternate control signals that include a bus switch signal that indicates whether a change in bus selection is to occur and a bus select signal that indicates which of the buses is to be selected, as required by claim 12.

Accordingly, it is respectfully submitted that claim 12 is not anticipated by Cranston et al. under 35 U.S.C. § 102. Reversal of the rejection of claim 12 is respectfully requested.

5. Claim 13.

Dependent claim 13 recites determining whether the control signals indicate that the buses are idle; and maintaining a previous bus selection when the control signals indicate that the buses are idle. Initially, claim 13 depends from claim 9 and is, therefore, not anticipated by Cranston et al. for at least the reasons that claim 9 is not anticipated.

Further, Cranston et al. does not disclose or suggest the combination of features recited in claim 13. For example, Cranston et al. does not disclose or suggest maintaining a previous bus selection when the control signals indicate that the buses are idle.

The Examiner alleged that Cranston et al. discloses this feature and cited column 8, lines 1-23, of Cranston et al. for support. Final Office Action, page 3. Appellant respectfully disagrees.

At column 8, lines 1-23, Cranston et al. discloses:

> The present embodiment preferably includes logic to implement the described methods in software modules as a set of computer executable software instructions. The Computer Processing Unit ("CPU") or microprocessor implements the logic that controls the operation of the channel card. The microprocessor executes software that can be programmed by those of skill in the art to provide the described functionality. The software can be represent as a sequence of binary bits maintained on a computer readable medium including magnetic disks, optical disks, organic disks, and any other volatile or (e.g., Random Access memory ("RAM")) non-volatile firmware (e.g., Read Only Memory ("ROM")) storage system readable by the CPU. The memory locations where data bits are maintained also include physical locations that have particular electrical, magnetic, optical, or organic properties corresponding to the stored data bits. The software instructions are executed as data bits by the CPU with a memory system causing a transformation of the electrical signal representation, and the maintenance of data bits at memory locations in the memory system to thereby reconfigure or otherwise alter the unit's operation. The executable software code may implement, for example, the methods described in further detail below.

In this section, Cranston et al. discloses that the invention may be embodied in software and

stored in a computer readable medium. Nowhere in this section, or elsewhere, however, does Cranston et al. disclose or suggest maintaining a previous bus selection when the control signals indicate that the buses are idle, as required by claim 13.

Accordingly, it is respectfully submitted that claim 13 is not anticipated by Cranston et al. under 35 U.S.C. § 102. Reversal of the rejection of claim 13 is respectfully requested.

6. Claim 15.

Dependent claim 15 recites that the control signals include a present signal that indicates whether a corresponding bus is operating and a master signal that indicates whether a corresponding bus is to be used. Initially, claim 15 depends from claim 9 and is, therefore, not anticipated by Cranston et al. for at least the reasons that claim 9 is not anticipated.

Further, Cranston et al. does not disclose or suggest the combination of features recited in claim 15. For example, Cranston et al. does not disclose or suggest control signals that include a present signal that indicates whether a corresponding bus is operating and a master signal that indicates whether a corresponding bus is to be used.

The Examiner alleged that Cranston et al. discloses these features and cited column 7, lines 7-56, of Cranston et al. for support. Final Office Action, page 4. Appellant respectfully disagrees.

At column 7, lines 7-56, Cranston et al. discloses that communication buses may be assigned priorities and selected based on the priorities, or assigned to classes where certain classes are allowed simultaneous access to an application card. Nowhere in this section, or elsewhere, however, does Cranston et al. disclose or suggest control signals that include a present signal that indicates whether a corresponding bus is operating and a master signal that indicates

whether a corresponding bus is to be used, as required by claim 15.

Accordingly, it is respectfully submitted that claim 15 is not anticipated by Cranston et al. under 35 U.S.C. § 102. Reversal of the rejection of claim 15 is respectfully requested.

7. Claim 16.

Dependent claim 16 recites that the control signals include a master signal that indicates whether a corresponding bus is to be used. Initially, claim 16 depends from claim 9 and is, therefore, not anticipated by Cranston et al. for at least the reasons that claim 9 is not anticipated.

Further, Cranston et al. does not disclose or suggest the combination of features recited in claim 16. For example, Cranston et al. does not disclose or suggest control signals that include a master signal that indicates whether a corresponding bus is to be used.

The Examiner alleged that Cranston et al. discloses this feature and cited column 7, lines 7-56, of Cranston et al. for support. Final Office Action, page 4. Appellant respectfully disagrees.

At column 7, lines 7-56, Cranston et al. discloses that communication buses may be assigned priorities and selected based on the priorities, or assigned to classes where certain classes are allowed simultaneous access to an application card. Nowhere in this section, or elsewhere, however, does Cranston et al. disclose or suggest control signals that include a master signal that indicates whether a corresponding bus is to be used, as required by claim 16.

Accordingly, it is respectfully submitted that claim 16 is not anticipated by Cranston et al. under 35 U.S.C. § 102. Reversal of the rejection of claim 16 is respectfully requested.

8. Claim 28.

Independent claim 28 is directed to a multi-bus system, comprising: a plurality of buses; a

plurality of master devices corresponding to the buses, each of the master devices controlling a corresponding one of the buses, the master devices generating control signals that indicate which of the buses is an active bus; and a plurality of slave devices connected to each of the buses and configured to receive the control signals, determine whether the control signals indicate that two or more of the buses are declared active buses, generate alternate control signals when the control signals indicate that two or more of the buses are declared active buses, and select one of the buses as the active bus using the alternate control signals.

Cranston et al. does not disclose or suggest the combination of features recited in claim 28. For example, Cranston et al. does not disclose or suggest a plurality of slave devices that, among other things, generate alternate control signals when control signals generated by the master devices indicate that two or more of the buses are declared active buses.

The Examiner alleged that Cranston et al. discloses these features and cited column 4, lines 40-67, and column 7, lines 7-56, of Cranston et al. for support. Final Office Action, page 4. Appellant respectfully disagrees.

At column 4, line 40 - column 5, line 2, Cranston et al. discloses:

> At any time, either of the management cards 26, 27 may initiate a communication or data transfer over its I^2C-bus to an application card using an I^2C-bus Start Sequence as described in more detail below. As a result, the application card receiving commands from the management cards via the I^2C-buses 18a, 18b must be able to dynamically switch between the two I^2C-bus interfaces to receive the data transfer. To select between the I^2C-buses, the application cards preferably include an arbiter that provides an interface to the I^2C-buses accessing the card and appropriately allows the active communication bus to access the application card.
>
> Referring now to FIG. 2, shown is a diagrammatic illustration of an application card 20 with an arbiter 50 that may be utilized to interface a plurality of incoming communication buses to the application card 20. The arbiter 50 also preferably implements and provides the selection between the plurality of mutually exclusive communication buses 18a, 18b having communication access to the application card 20. The active communication bus

> carrying communications for the application card will access the devices on the application card through a local bus (Local Data and Local Clock), which may also include an I^2C-bus. As shown in the example of FIG. 2, a plurality of communication buses, Bus A and Bus B 18a, 18b in this example, access the application card 20. Thus, the application card 20 may receive messages from either of the communication buses, Bus A or B. The arbiter 50 determines which of the communication buses 18a, 18b the application card 20 (at Local Card Data and Local Card Clock) will receive messages from using methods described in more detail below.

In this section, Cranston et al. discloses that an application card includes an arbiter that selects between a plurality of communication buses to identify from which communication bus the application card will receive messages. Nowhere in this section, or elsewhere, does Cranston et al. disclose or suggest that the application cards generate alternate control signals when control signals generated by master devices indicate that two or more of the buses are declared active buses, as required by claim 28.

At column 7, lines 7-56, Cranston et al. discloses that communication buses may be assigned priorities and selected based on the priorities, or assigned to classes where certain classes are allowed simultaneous access to an application card. Nowhere in this section, or elsewhere, however, does Cranston et al. disclose or suggest slave devices that generate alternate control signals when control signals generated by master devices indicate that two or more of the buses are declared active buses, as required by claim 28.

Because Cranston et al. does not disclose or suggest slave devices that generate alternate control signals when control signals generated by master devices indicate that two or more of the buses are declared active buses, Cranston et al. cannot disclose or suggest that the slave devices select one of the buses as the active bus using the alternate control signals, as further recited in claim 28.

Accordingly, it is respectfully submitted that claim 28 is not anticipated by Cranston et al.

under 35 U.S.C. § 102. Reversal of the rejection of claim 28 is respectfully requested.

B. Rejection Under 35 U.S.C. § 103(a) Over Jaramillo et al. (U.S. Patent No. 6,598,104) in View of Wang et al. (U.S. Patent Application Publication No. (US 2004/0098525).

1. Claims 1, 5, and 7.

The initial burden of establishing a prima facie basis to deny patentability to a claimed invention is always upon the Examiner. In re Oetiker, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In rejecting a claim under 35 U.S.C. § 103, the Examiner must provide a factual basis to support the conclusion of obviousness. In re Warner, 379 F.2d 1011, 154 USPQ 173 (CCPA 1967). Based upon the objective evidence of record, the Examiner is required to make the factual inquiries mandated by Graham v. John Deere Co., 86 S.Ct. 684, 383 U.S. 1, 148 USPQ 459 (1966). The Examiner is also required to explain how and why one having ordinary skill in the art would have been led to modify an applied reference and/or combine applied references to arrive at the claimed invention. Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 5 USPQ2d 1434 (Fed. Cir. 1988).

In establishing motivation, it has been consistently held that the requisite motivation to support the conclusion of obviousness is not an abstract concept, but must stem from the prior art as a whole to impel one having ordinary skill in the art to modify a reference or combine references with a reasonable expectation of successfully achieving some particular realistic objective. See, for example, Interconnect Planning Corp. v. Feil, 227 F.2d 1132, 227 USPQ 543 (Fed. Cir. 1985).

With these principles in mind, Appellant submits that independent claim 1 is patentable

over Jaramillo et al. and Wang et al. Independent claim 1 is directed to a system for selecting bus mastership in a multi-master system. The system comprises a plurality of master devices and a plurality of slave devices connected to the master devices via a bus. The master devices are configured to generate control signals relating to control of the bus in the multi-master system. Each of the slave devices is configured to receive the control signals from the master devices, determine whether a conflict in the control signals exists, generate one or more alternate control signals for selecting bus mastership when a conflict is determined to exist, and determine which of the master devices obtains control of the bus using the one or more alternate control signals when a conflict is determined to exist.

Neither Jaramillo et al. nor Wang et al., whether taken alone or in any reasonable combination, discloses or suggests the combination of features recited in claim 1. For example, neither Jaramillo et al. nor Wang et al. discloses or suggests a slave device that is configured to, among other things, determine whether a conflict exists in control signals received from master devices that relate to control of a bus.

The Examiner alleged that PCI initiators 402-404 correspond to the plurality of master devices recited in claim 1 and PCI target agent 405 corresponds to the plurality of slave devices recited in claim 1. Final Office Action, page 12. The Examiner alleged that Jaramillo et al. discloses a slave device that determines whether a conflict exists based on control signals and cited column 5, lines 52-62, of Jaramillo et al. for support. Final Office Action, page 5. Appellant respectfully disagrees.

At column 5, lines 52-62, Jaramillo et al. discloses:

FIG. 3 shows a block diagram of a smart retry access process 300 utilized in accordance

> with one embodiment of the present invention. On the left side of process 300 in step 301, a PCI initiator agent accesses a PCI target agent and attempts a data transmission. The initial access is comprised of the normal stages of a PCI transaction (e.g., arbitration for PCI bus ownership, receiving a grant signal from a PCI arbiter, addressing and informing a PCI target agent of the data to be transferred, etc.). In step 302 the PCI target agent issues a retry in instances where the PCI target agent is busy and cannot complete the data transaction.

In this section, Jaramillo et al. discloses that a PCI initiator agent (master) accesses a PCI target agent (slave) and attempts a data transmission, which involves arbitrating for PCI bus ownership, receiving a grant signal from the PCI arbiter, and informing the PCI target agent of the data to be transferred, and the PCI target agent issues a retry when the PCI target agent is busy. Nowhere in this section, or elsewhere, does Jaramillo et al. disclose or suggest that a slave device (PCI target agent) determines whether a conflict exists in control signals received from master devices (PCI initiator agents) that relate to control of a bus, as required by claim 1.

In other words, Jaramillo et al. does not disclose or suggest that a PCI target agent determines whether a conflict exists in control signals received from the PCI initiator agents that relate to control of a bus. Instead, PCI target agent issues a retry which denies the PCI initiator agent bus access when the PCI target agent is busy with an internal activity, engaging in a transaction that would generate a conflict, or will be slowed in completing a transaction. Column 8, lines 57-61. While Jaramillo et al. discloses that a PCI target agent issues a retry when engaging in a transaction that would generate a conflict, Jaramillo et al. does not disclose or suggest determining whether a conflict exists in control signals received from master devices that relate to control of a bus, as required by claim 1. Further, Jaramillo et al. discloses that denying the PCI initiator agent bus access permits the PCI bus to be available for use by other PCI initiator agents. Column 5, line 66 - column 6, line 1. Therefore, any conflict in the PCI target

agent has nothing to do with a conflict in control signals from master devices that relate to control of the bus.

Further, Jaramillo et al. clearly discloses that a PCI initiator agent communicates with a PCI target agent only after the PCI initiator agent is granted access to the bus by the PCI arbiter. Column 5, lines 57-59; column 8, lines 49-52. Jaramillo et al. discloses that the PCI arbiter handles requests for PCI bus ownership. Column 5, lines 57-59; column 8, lines 49-52. Therefore, the PCI target agent is not involved in requests for PCI bus ownership.

In addition, neither Jaramillo et al. nor Wang et al., whether taken alone or in any reasonable combination, discloses or suggests a slave device that is configured to generate one or more alternate control signals for selecting bus mastership when a conflict in control signals received from the master devices is determined to exist, as further recited in claim 1.

The Examiner alleged that Jaramillo et al. discloses generating one or more alternate control signals for selecting bus mastership when a conflict is determined to exist and cited column 5, line 52 - column 7, line 18, of Jaramillo et al. for support. Final Office Action, page 5. Appellant respectfully disagrees.

At column 5, line 52 - column 7, line 18, Jaramillo et al. discloses that a PCI initiator agent accesses a PCI target agent and attempts a data transmission and the PCI target agent issues a retry in instances where the PCI target agent is busy and cannot complete the data transmission. During this time, Jaramillo et al. discloses that the PCI arbiter masks requests for the bus from the PCI initiator agent. Column 9, lines 6-15. When the PCI target agent is no longer busy, it signals the PCI arbiter to grant PCI bus access to the PCI initiator agent. Column 6, lines 11-13. Nowhere in this section, or elsewhere, does Jaramillo et al. disclose or suggest that a slave device

(PCI target agent) generates one or more alternate control signals for selecting bus mastership when a conflict is determined to exist, as required by claim 1.

The Examiner also alleged that Jaramillo et al. discloses that the PCI target agent includes the ability to access a second signal, which the Examiner alleged was the equivalent of an alternate control signal, indicating the grant status of the PCI bus. Final Office Action, page 12. Appellant respectfully disagrees.

At column 6, lines 58 - column 7, line 2, Jaramillo et al. discloses:

> PCI target agent 405 of the present embodiment includes the ability to access a second signal (hereinafter referred to as the PCI bus grant signal) indicating the grant status of the PCI bus 406. It should appreciated that the PCI bus grant signal is communicated via the grant bus gnt_n (2:0) 502 shown in FIG. 5. The grant bus gnt_n (2:0) 502 is snooped by PCI initiator agents 402, 403 and 404 and, in accordance with the present embodiment, the grant bus gnt_n (2:0) 502 is also snooped by PCI target agent 405. By snooping the grant bus gnt_n (2:0) 502 the PCI target agent 405 can determine which PCI initiator agent is trying to access it.

Even assuming, for the sake of argument, that the PCI bus grant signal (second signal) could be equated to an alternate control signal (a point that Appellant does not concede), Jaramillo et al. does not disclose or suggest that the PCI bus grant signal is generated by a slave device, as would be required by claim 1. Instead, Jaramillo et al. discloses that the PCI bus grant signal is generated by the PCI arbiter and only snooped by the PCI target agent. Figure 5; column 6, lines 11-16 and 64-67.

In addition, neither Jaramillo et al. nor Wang et al. discloses or suggests a slave device that is configured to determine which of the master devices obtains control of the bus using one or more alternate control signals generated when a conflict is determined to exist, as required by claim 1. The Examiner admitted that Jaramillo et al. does not disclose this feature and relied on Wang et al. for allegedly disclosing the feature and cited paragraph 0027 of Wang et al. for

support. Final Office Action, page 6. Appellant respectfully disagrees.

At paragraph 0027, Wang et al. discloses:

> The arbiter 310 arbitrates the access requests from the N master processors via the N master buses. The arbiter 310 generates arbitration signals as result of the arbitration. The arbitration signals indicate which master processor is given access to the slave device if there is access conflict. The corresponding master processors are informed of the arbitration so that it can proceed with the access if the access is granted, or attempt to access again if the access is denied.

The arbiter that Wang et al. refers to in this section is a part of the system bus controller illustrated in Figure 1. Nowhere in this section, or elsewhere, does Wang et al. disclose or suggest that a slave device is configured to determine which of the master devices obtains control of the bus using one or more alternate control signals generated by the slave device when a conflict exists in control signals relating to control of the bus from the master devices, as required by claim 1.

Accordingly, it is respectfully submitted that claim 1 is patentable over Jaramillo et al. and Wang et al., whether taken alone or in any reasonable combination, under 35 U.S.C. § 103. Reversal of the rejection of claim 1 is respectfully requested.

2. Claim 2.

Dependent claim 2 recites bus selection logic that is configured to determine whether the control signals indicate that two or more of the master devices concurrently assert control of the bus and generate a conflict indication signal when two or more of the master devices concurrently assert control of the bus, and conflict resolution logic that is configured to generate the one or more alternate control signals in response to the conflict indication signal. Initially, claim 2 depends from claim 1 and is, therefore, patentable over Jaramillo et al. and Wang et al.

for at least the reasons that claim 1 is patentable.

Further, neither Jaramillo et al. nor Wang et al., whether taken alone or in any reasonable combination, discloses or suggests the combination of features recited in claim 2. For example, neither Jaramillo et al. nor Wang et al. discloses or suggests bus selection logic that is configured to determine whether the control signals indicate that two or more of the master devices concurrently assert control of the bus and generate a conflict indication signal when two or more of the master devices concurrently assert control of the bus.

The Examiner alleged that Jaramillo et al. discloses bus selection logic and cited column 5, line 52 - column 6, line 40, of Jaramillo et al. for support. Final Office Action, page 6. Appellant respectfully disagrees.

At column 5, line 52 - column 6, line 40, Jaramillo et al. discloses that a PCI initiator agent accesses a PCI target agent and attempts a data transmission and the PCI target agent issues a retry in instances where the PCI target agent is busy and cannot complete the data transmission. When the PCI target agent is no longer busy, it signals the PCI arbiter to grant PCI bus access to the PCI initiator agent. Nowhere in this section, or elsewhere, does Jaramillo et al. disclose or suggest bus selection logic of a slave device that determines whether the control signals indicate that two or more of the master devices concurrently assert control of the bus, as recited in claim 2.

Instead, Jaramillo et al. discloses that a PCI target agent issues a retry when the PCI target agent is busy and cannot complete a transaction. Column 5, lines 60-62. Jaramillo et al. is concerned with PCI target agent availability and not bus conflicts as evident by the fact that Jaramillo et al. discloses that a PCI initiator agent that has received a retry signal from one PCI

target agent can access the bus for purposes of communicating with other PCI target agents. Column 6, lines 33-40.

Further, Jaramillo et al. clearly discloses that a PCI initiator agent communicates with a PCI target agent only after the PCI initiator agent is granted access to the bus by the PCI arbiter. Column 5, lines 57-59; column 8, lines 49-52. Jaramillo et al. discloses that the PCI arbiter handles requests for PCI bus ownership. Column 5, lines 57-59; column 8, lines 49-52. Therefore, the PCI target agent is not involved in requests for PCI bus ownership.

The Examiner also alleged that Jaramillo et al. discloses that a PCI target agent includes the ability to access a second signal (which the Examiner alleged is equivalent to an alternate control signal) indicating the grant status of the PCI bus. Final Office Action, page 13. Jaramillo et al. discloses that this "second" signal (i.e., PCI bus grant signal) indicates which PCI initiator agent is granted access to the bus. Nowhere does Jaramillo et al. disclose or suggest that the PCI target agent (slave device) uses the PCI bus grant signal to determine whether control signals indicate that two or more of the PCI initiator agents (master devices) concurrently assert control of the bus, but instead indicates to the PCI target agent which of the PCI initiator agents is currently granted bus access.

Accordingly, it is respectfully submitted that claim 2 is patentable over Jaramillo et al. and Wang et al., whether taken alone or in any reasonable combination, under 35 U.S.C. § 103. Reversal of the rejection of claim 2 is respectfully requested.

3. Claim 6.

Dependent claim 6 recites that the control signals include a present signal that indicates whether a corresponding one of the master devices is operating and a master signal that indicates

whether a corresponding one of the master devices asserts control of the bus. Initially, claim 6 depends from claim 1 and is, therefore, patentable over Jaramillo et al. and Wang et al. for at least the reasons that claim 1 is patentable.

Further, neither Jaramillo et al. nor Wang et al., whether taken alone or in any reasonable combination, discloses or suggests the combination of features recited in claim 6. For example, neither Jaramillo et al. nor Wang et al. discloses or suggests control signals that include a present signal that indicates whether a corresponding one of the master devices is operating and a master signal that indicates whether a corresponding one of the master devices asserts control of the bus.

The Examiner alleged that Jaramillo et al. discloses a present signal and a master signal and cited column 5, line 52 - column 6, line 40, of Jaramillo et al. for support. Final Office Action, page 8. Appellant respectfully disagrees.

Contrary to the Examiner's allegation, nowhere in column 5, line 52 - column 6, line 40, or elsewhere, does Jaramillo et al. disclose or suggest anything resembling control signals that include a present signal that indicates whether a corresponding one of the master devices is operating and a master signal that indicates whether a corresponding one of the master devices asserts control of the bus, as required by claim 6. Moreover, the Examiner has not explained how the above section of Jaramillo et al. can reasonably be construed to disclose the present and master signals.

Accordingly, it is respectfully submitted that claim 6 is patentable over Jaramillo et al. and Wang et al., whether taken alone or in any reasonable combination, under 35 U.S.C. § 103. Reversal of the rejection of claim 6 is respectfully requested.

4. Claims 8 and 17.

Independent claim 8, for example, is directed to a system for selecting a master in a multi-master system. The system comprises means for outputting first and second control signals relating to mastership in the multi-master system from each of a plurality of masters in the multi-master system, means for determining whether a conflict for mastership exists based on the first and second control signals, means for generating a switch signal and a select signal when a conflict is determined to exist, and means for selecting one of the masters using the switch signal and the select signal.

Neither Jaramillo et al. nor Wang et al., whether taken alone or in any reasonable combination, discloses or suggests the combination of features recited in claim 8. For example, neither Jaramillo et al. nor Wang et al. discloses or suggests means for outputting first and second control signals relating to mastership in the multi-master system from each of a plurality of masters in the multi-master system. The Examiner alleged that Jaramillo et al. discloses means for outputting first and second control signals relating to mastership and cited column 5, lines 52-62, of Jaramillo et al. for support. Final Office Action, page 8. Appellant respectfully disagrees.

Column 5, lines 52-62, of Jaramillo et al. has been reproduced above. In this section, Jaramillo et al. discloses that a PCI initiator agent (master) accesses a PCI target agent (slave) and attempts a data transmission, which involves arbitrating for PCI bus ownership, receiving a grant signal from the PCI arbiter, and informing the PCI target agent of the data to be transferred, and the PCI target agent issues a retry when the PCI target agent is busy. Nowhere in this section, or elsewhere, does Jaramillo et al. disclose or suggest means for outputting first and second control signals relating to mastership in the multi-master system from each of a plurality

of masters in the multi-master system, as required by claim 8.

In addition, neither Jaramillo et al. nor Wang et al. discloses or suggests means for generating a switch signal and a select signal when a conflict for mastership is determined to exist, as further recited in claim 8. The Examiner alleged that Jaramillo et al. discloses this feature and cited column 5, line 52 - column 6, line 40, of Jaramillo et al. for support. Final Office Action, page 9. Appellant respectfully disagrees.

At column 5, line 52 - column 6, line 40, Jaramillo et al. discloses that a PCI initiator agent attempts to perform a data transaction with a PCI target agent and the PCI target agent issues a retry when the PCI target agent is busy and cannot complete the data transaction. Nowhere in this section, or elsewhere, does Jaramillo et al. disclose or suggest means for generating a switch signal and a select signal when a conflict for mastership is determined to exist, as required by claim 8.

Accordingly, it is respectfully submitted that claim 8 is patentable over Jaramillo et al. and Wang et al., whether taken alone or in any reasonable combination, under 35 U.S.C. § 103. Reversal of the rejection of claim 8 is respectfully requested.

5. Claims 18 and 21.

Independent claim 18 recites that in a multi-master system comprising a plurality of master devices connected to a plurality of slave devices, each of the slave devices comprises selection logic configured to determine whether control signals from the master devices indicate that two or more of the master devices concurrently assert mastership within the multi-master system, generate a conflict indication signal when two or more of the master devices concurrently assert mastership, and select mastership using one or more alternate control signals when two or

more of the master devices concurrently assert mastership; and conflict resolution logic configured to generate the one or more alternate control signals to identify mastership in response to the conflict indication signal.

Neither Jaramillo et al. nor Wang et al., whether taken alone or in any reasonable combination, discloses or suggests the combination of features recited in claim 18. For example, neither Jaramillo et al. nor Wang et al. discloses or suggests a slave device that includes selection logic configured to, among other things, determine whether control signals from the master devices indicate that two or more of the master devices concurrently assert mastership within the multi-master system.

The Examiner alleged that PCI initiators 402-404 correspond to the plurality of master devices recited in claim 18 and PCI target agent 405 corresponds to the plurality of slave devices recited in claim 18. Final Office Action, page 12. The Examiner alleged that Jaramillo et al. discloses a slave device that determines whether a conflict exists based on control signals and cited column 5, lines 52-62, of Jaramillo et al. for support. Final Office Action, page 5. Appellant respectfully disagrees.

Column 5, lines 52-62, of Jaramillo et al. has been reproduced above. In this section, Jaramillo et al. discloses that a PCI initiator agent (master) accesses a PCI target agent (slave) and attempts a data transmission, which involves arbitrating for PCI bus ownership, receiving a grant signal from the PCI arbiter, and informing the PCI target agent of the data to be transferred, and the PCI target agent issues a retry when the PCI target agent is busy. Nowhere in this section, or elsewhere, does Jaramillo et al. disclose or suggest that a slave device (PCI target agent) includes selection logic configured to determine whether control signals from the master

devices (PCI initiator agents) indicate that two or more of the master devices concurrently assert mastership within the multi-master system, as required by claim 18.

In other words, Jaramillo et al. does not disclose or suggest that a PCI target agent includes selection logic to determine whether control signals from the PCI initiator agents indicate that two or more of the PCI initiator agents concurrently assert mastership. Instead, a PCI target agent issues a retry which denies the PCI initiator agent bus access when the PCI target agent is busy with an internal activity, engaging in a transaction that would generate a conflict, or will be slowed in completing a transaction. Column 8, lines 57-61. While Jaramillo et al. discloses that a PCI target agent issues a retry when engaging in a transaction that would generate a conflict, Jaramillo et al. does not disclose or suggest determining whether control signals from the master devices indicate that two or more of the master devices concurrently assert mastership, as required by claim 18.

Further, Jaramillo et al. clearly discloses that a PCI initiator agent communicates with a PCI target agent only after the PCI initiator agent is granted access to the bus by the PCI arbiter. Column 5, lines 57-59; column 8, lines 49-52. Jaramillo et al. discloses that the PCI arbiter handles requests for PCI bus ownership. Column 5, lines 57-59; column 8, lines 49-52.

In addition, neither Jaramillo et al. nor Wang et al., whether taken alone or in any reasonable combination, discloses or suggests a slave device that includes conflict resolution logic that is configured to generate one or more alternate control signals to identify mastership in response to a conflict indication signal generated by the selection logic, as further recited in claim 18.

The Examiner alleged that Jaramillo et al. discloses generating one or more alternate

control signals for selecting bus mastership when a conflict is determined to exist and cited column 5, line 52 - column 7, line 18, of Jaramillo et al. for support. Final Office Action, page 5. Appellant respectfully disagrees.

At column 5, line 52 - column 7, line 18, Jaramillo et al. discloses that a PCI initiator agent accesses a PCI target agent and attempts a data transmission and the PCI target agent issues a retry in instances where the PCI target agent is busy and cannot complete the data transmission. During this time, Jaramillo et al. discloses that the PCI arbiter masks requests for the bus from the PCI initiator agent. Column 9, lines 6-15. When the PCI target agent is no longer busy, it signals the PCI arbiter to grant PCI bus access to the PCI initiator agent. Column 6, lines 11-13. Nowhere in this section, or elsewhere, does Jaramillo et al. disclose or suggest that a slave device (PCI target agent) includes conflict resolution logic that is configured to generate one or more alternate control signals to identify mastership in response to a conflict indication signal generated by the selection logic, as required by claim 18.

The Examiner also alleged that Jaramillo et al. discloses that the PCI target agent includes the ability to access a second signal, which the Examiner alleged was the equivalent of an alternate control signal, indicating the grant status of the PCI bus. Final Office Action, page 12. Appellant respectfully disagrees.

At column 6, lines 58 - column 7, line 2, Jaramillo et al. discloses:

> PCI target agent 405 of the present embodiment includes the ability to access a second signal (hereinafter referred to as the PCI bus grant signal) indicating the grant status of the PCI bus 406. It should appreciated that the PCI bus grant signal is communicated via the grant bus gnt_n (2:0) 502 shown in FIG. 5. The grant bus gnt_n (2:0) 502 is snooped by PCI initiator agents 402, 403 and 404 and, in accordance with the present embodiment, the grant bus gnt_n (2:0) 502 is also snooped by PCI target agent 405. By snooping the grant bus gnt_n (2:0) 502 the PCI target agent 405 can determine which PCI initiator agent is trying to access it.

Even assuming, for the sake of argument, that the PCI bus grant signal (second signal) could be equated to an alternate control signal (a point that Appellant does not concede), Jaramillo et al. does not disclose or suggest that the PCI bus grant signal is generated by a slave device, as would be required by claim 18. Instead, Jaramillo et al. discloses that the PCI bus grant signal is generated by the PCI arbiter and only snooped by the PCI target agent. Figure 5; column 6, lines 11-16 and 64-67.

In addition, neither Jaramillo et al. nor Wang et al. discloses or suggests a slave device that includes selection logic that is configured to select mastership using the one or more alternate control signals from the conflict resolution logic when two or more of the master devices concurrently assert mastership, as required by claim 18. The Examiner admitted that Jaramillo et al. does not disclose this feature and relied on Wang et al. for allegedly disclosing the feature and cited paragraph 0027 of Wang et al. for support. Final Office Action, page 6. Appellant respectfully disagrees.

At paragraph 0027, Wang et al. discloses:

> The arbiter 310 arbitrates the access requests from the N master processors via the N master buses. The arbiter 310 generates arbitration signals as result of the arbitration. The arbitration signals indicate which master processor is given access to the slave device if there is access conflict. The corresponding master processors are informed of the arbitration so that it can proceed with the access if the access is granted, or attempt to access again if the access is denied.

The arbiter that Wang et al. refers to in this section is a part of the system bus controller illustrated in Figure 1. Nowhere in this section, or elsewhere, does Wang et al. disclose or suggest a slave device that includes selection logic that is configured to select mastership using the one or more alternate control signals from the conflict resolution logic when two or more of

the master devices concurrently assert mastership, as required by claim 18.

Accordingly, it is respectfully submitted that claim 18 is patentable over Jaramillo et al. and Wang et al., whether taken alone or in any reasonable combination, under 35 U.S.C. § 103. Reversal of the rejection of claim 18 is respectfully requested.

6. Claim 20.

Dependent claim 20 recites that the control signals include a present signal that indicates whether a corresponding one of the master devices is operating and a master signal that indicates whether a corresponding one of the master devices asserts mastership. Initially, claim 20 depends from claim 18 and is, therefore, patentable over Jaramillo et al. and Wang et al. for at least the reasons that claim 18 is patentable.

Further, neither Jaramillo et al. nor Wang et al., whether taken alone or in any reasonable combination, discloses or suggests the combination of features recited in claim 20. For example, neither Jaramillo et al. nor Wang et al. discloses or suggests control signals that include a present signal that indicates whether a corresponding one of the master devices is operating and a master signal that indicates whether a corresponding one of the master devices asserts mastership.

The Examiner alleged that Jaramillo et al. discloses a present signal and a master signal and cited column 5, line 52 - column 6, line 40, of Jaramillo et al. for support. Final Office Action, page 8. Appellant respectfully disagrees.

At column 5, line 52 - column 6, line 40, Jaramillo et al. discloses that a PCI initiator agent attempts to perform a data transaction with a PCI target agent and the PCI target agent issues a retry when the PCI target agent is busy and cannot complete the data transaction. Contrary to the Examiner's allegation, nowhere in column 5, line 52 - column 6, line 40, or

elsewhere, does Jaramillo et al. disclose or suggest anything resembling control signals that include a present signal that indicates whether a corresponding one of the master devices is operating and a master signal that indicates whether a corresponding one of the master devices asserts mastership, as required by claim 20.

Accordingly, it is respectfully submitted that claim 20 is patentable over Jaramillo et al. and Wang et al., whether taken alone or in any reasonable combination, under 35 U.S.C. § 103. Reversal of the rejection of claim 20 is respectfully requested.

7. Claims 23 and 26.

Independent claim 23 is directed to a method for selecting bus mastership in a multi-master system comprising a plurality of master devices connected to a plurality of slave devices via at least one bus. The method, performed by each of the slave devices, comprises determining whether control signals from the master devices indicate that two or more of the master devices concurrently assert bus mastership; generating one or more alternate control signals to identify which of the master devices obtains bus mastership when two or more of the master devices concurrently assert bus mastership; determining which of the master devices obtains bus mastership using the one or more alternate control signals when two or more of the master devices concurrently assert bus mastership; and determining which of the master devices obtains bus mastership using the control signals when one of the master devices asserts bus mastership.

Neither Jaramillo et al. nor Wang et al., whether taken alone or in any reasonable combination, discloses or suggests the combination of features recited in claim 23. For example, neither Jaramillo et al. nor Wang et al. discloses or suggests determining, by a slave device, whether control signals from the master devices indicate that two or more of the master devices

concurrently assert bus mastership.

The Examiner alleged that PCI initiators 402-404 correspond to the plurality of master devices recited in claim 23 and PCI target agent 405 corresponds to the plurality of slave devices recited in claim 23. Final Office Action, page 12. The Examiner alleged that Jaramillo et al. discloses determining whether control signals from the master devices indicate that two or more of the master devices concurrently assert bus mastership and cited column 6, lines 17-39, of Jaramillo et al. for support. Final Office Action, page 7. Appellant respectfully disagrees.

At column 6, lines 17-39, Jaramillo et al. discloses:

> It should be appreciated that the present embodiment relies on a PCI initiator agent attempting to access only one PCI target agent at a time. It should be further appreciated that in the preferred embodiment, when a PCI target agent issues a retry, the PCI initiator agent repeatedly requests the PCI bus for purposes of accessing the same PCI target agent. The PCI initiator agent does this until it completes a transaction with the PCI target agent that issued the retry, before attempting to access any other PCI target agents. PCI systems typically behave in this manner. That is, if a retry is issued the PCI initiator agent continually retries to access the same PCI target agent before attempting to access any other PCI target agents.
>
> It should be appreciated the present invention can be adapted by one skilled in the art to accommodate other configurations of a PCI system. For example, when a PCI target agent signals a PCI initiator agent to retry later, the PCI initiator agent can access the PCI bus for purposes of communicating with other PCI target agents. However, unless the PCI target agent is ready, the PCI initiator agent can not access the PCI bus for purposes of communicating with the PCI target agent that issued the retry.

In this section, Jaramillo et al. discloses that when a PCI target agent issues a retry to a PCI initiator agent, the PCI initiator agent repeatedly requests the bus so that it can access the same PCI target agent, or the PCI initiator agent can request the bus for accessing another PCI target agent. Nowhere in this section, or elsewhere, does Jaramillo et al. disclose or suggest determining, by a slave device (PCI target agent), whether control signals from the master devices (PCI initiator agents) indicate that two or more of the master devices concurrently assert

bus mastership, as required by claim 23.

In other words, Jaramillo et al. does not disclose or suggest that a PCI target agent determines whether control signals from the PCI initiator agents indicate that two or more of the PCI initiator agents concurrently assert bus mastership. Instead, a PCI target agent issues a retry that denies the PCI initiator agent bus access when the PCI target agent is busy with an internal activity, engaging in a transaction that would generate a conflict, or will be slowed in completing a transaction. Column 8, lines 57-61. While Jaramillo et al. discloses that a PCI target agent issues a retry when engaging in a transaction that would generate a conflict, Jaramillo et al. does not disclose or suggest determining, by a slave device, whether control signals from the master devices indicate that two or more of the master devices concurrently assert bus mastership, as required by claim 23.

Further, Jaramillo et al. clearly discloses that a PCI initiator agent communicates with a PCI target agent only after the PCI initiator agent is granted access to the bus by the PCI arbiter. Column 5, lines 57-59; column 8, lines 49-52. Jaramillo et al. discloses that the PCI arbiter handles requests for PCI bus ownership. Column 5, lines 57-59; column 8, lines 49-52. Therefore, the PCI target agent would not be involved in requests for PCI bus ownership.

In addition, neither Jaramillo et al. nor Wang et al., whether taken alone or in any reasonable combination, discloses or suggests generating, by a slave device, one or more alternate control signals to identify which of the master devices obtains bus mastership when two or more of the master devices concurrently assert bus mastership, as further recited in claim 23.

The Examiner alleged that Jaramillo et al. discloses generating one or more alternate control signals and cited column 6, line 18 - column 7, line 18, of Jaramillo et al. for support.

Final Office Action, page 7. Appellant respectfully disagrees.

At column 6, line 18 - column 7, line 18, Jaramillo et al. discloses that a PCI initiator agent accesses a PCI target agent and attempts a data transmission and the PCI target agent issues a retry in instances where the PCI target agent is busy and cannot complete the data transmission. During this time, Jaramillo et al. discloses that the PCI arbiter masks requests for the bus from the PCI initiator agent. Column 9, lines 6-15. When the PCI target agent is no longer busy, it signals the PCI arbiter to grant PCI bus access to the PCI initiator agent. Column 6, lines 11-13. Nowhere in this section, or elsewhere, does Jaramillo et al. disclose or suggest generating, by a slave device (PCI target agent) one or more alternate control signals to identify which of the master devices (PCI initiator agents) obtains bus mastership when two or more of the master devices concurrently assert bus mastership, as required by claim 23.

In addition, neither Jaramillo et al. nor Wang et al. discloses or suggests determining, by a slave device, which of the master devices obtains bus mastership using the one or more alternate control signals when two or more of the master devices concurrently assert bus mastership, as required by claim 23. The Examiner admitted that Jaramillo et al. does not disclose this feature and relied on Wang et al. for allegedly disclosing the feature and cited paragraph 0027 of Wang et al. for support. Final Office Action, page 7. Appellant respectfully disagrees.

At paragraph 0027, Wang et al. discloses:

> The arbiter 310 arbitrates the access requests from the N master processors via the N master buses. The arbiter 310 generates arbitration signals as result of the arbitration. The arbitration signals indicate which master processor is given access to the slave device if there is access conflict. The corresponding master processors are informed of the arbitration so that it can proceed with the access if the access is granted, or attempt to access again if the access is denied.

The arbiter that Wang et al. refers to in this section is a part of the system bus controller illustrated in Figure 1. Nowhere in this section, or elsewhere, does Wang et al. disclose or suggest determining, by a slave device, which of the master devices obtains bus mastership using the one or more alternate control signals when two or more of the master devices concurrently assert bus mastership, as required by claim 23.

Accordingly, it is respectfully submitted that claim 23 is patentable over Jaramillo et al. and Wang et al., whether taken alone or in any reasonable combination, under 35 U.S.C. § 103. Reversal of the rejection of claim 23 is respectfully requested.

8. Claim 25.

Dependent claim 25 recites that the control signals include a present signal that indicates whether a corresponding one of the master devices is operating and a master signal that indicates whether a corresponding one of the master devices asserts bus mastership. Initially, claim 25 depends from claim 23 and is, therefore, patentable over Jaramillo et al. and Wang et al. for at least the reasons that claim 23 is patentable.

Further, neither Jaramillo et al. nor Wang et al., whether taken alone or in any reasonable combination, discloses or suggests the combination of features recited in claim 25. For example, neither Jaramillo et al. nor Wang et al. discloses or suggests control signals that include a present signal that indicates whether a corresponding one of the master devices is operating and a master signal that indicates whether a corresponding one of the master devices asserts bus mastership.

The Examiner alleged that Jaramillo et al. discloses a present signal and a master signal and cited column 5, line 52 - column 6, line 40, of Jaramillo et al. for support. Final Office Action, page 8. Appellant respectfully disagrees.

At column 5, line 52 - column 6, line 40, Jaramillo et al. discloses that a PCI initiator agent attempts to perform a data transaction with a PCI target agent and the PCI target agent issues a retry when the PCI target agent is busy and cannot complete the data transaction. Contrary to the Examiner's allegation, nowhere in column 5, line 52 - column 6, line 40, or elsewhere, does Jaramillo et al. disclose or suggest anything resembling control signals that include a present signal that indicates whether a corresponding one of the master devices is operating and a master signal that indicates whether a corresponding one of the master devices asserts bus mastership, as required by claim 25.

Accordingly, it is respectfully submitted that claim 25 is patentable over Jaramillo et al. and Wang et al., whether taken alone or in any reasonable combination, under 35 U.S.C. § 103. Reversal of the rejection of claim 25 is respectfully requested.

9. Claim 27.

Independent claim 27 is directed to a multi-master system that comprises a plurality of master devices, conflict resolution logic, and a plurality of slave devices. The master devices are configured to generate control signals relating to bus mastership. The conflict resolution logic is configured to receive the control signals from the master devices, determine whether the control signals indicate that two or more of the master devices concurrently assert bus mastership, and generate a switch signal and a select signal when it is determined that two or more of the master devices concurrently assert bus mastership. The slave devices are configured to select bus mastership using the switch signal and the select signal when the control signals indicate that two or more of the master devices concurrently assert bus mastership.

Initially, Appellant submits that the Examiner's rejection of claim 27 is improper. For

example, the Examiner rejected claim 27 based on a combination of Jaramillo et al. and Wang et al. In the rejection of the features of claim 27, however, the Examiner relied only on the Jaramillo et al. reference for allegedly disclosing every feature of claim 27. The Examiner cited no portion of Wang et al. and provided no motivation for combining the alleged features of Jaramillo et al. and Wang et al. Therefore, the Examiner's rejection of claim 27 based on a combination of Jaramillo et al. and Wang et al. is improper.

Nevertheless, neither Jaramillo et al. nor Wang et al., whether taken alone or in any reasonable combination, discloses or suggests the combination of features recited in claim 27. For example, neither Jaramillo et al. nor Wang et al. discloses or suggests conflict resolution logic that is configured to, among other things, generate a switch signal and a select signal when it is determined that two or more of the master devices concurrently assert bus mastership.

The Examiner alleged that Jaramillo et al. discloses these features and cited column 6, line 18 - column 7, line 18, of Jaramillo et al. for support. Final Office Action, page 9. Appellant respectfully disagrees.

At column 6, line 18 - column 7, line 18, Jaramillo et al. discloses that when a PCI initiator agent attempts to access a PCI target agent, the PCI target agent issues a bus denial signal to the PCI arbiter so that the PCI arbiter will deny the PCI initiator agent bus access. Nowhere in this section, or elsewhere, does Jaramillo et al. disclose conflict resolution logic that generates a switch signal and a select signal when it is determined that two or more master devices concurrently assert bus mastership, as required by claim 27.

In addition, neither Jaramillo et al. nor Wang et al. discloses or suggests a plurality of slave devices that are configured to select bus mastership using the switch signal and the select

signal when the control signals indicate that two or more of the master devices concurrently assert bus mastership, as further recited in claim 27. The Examiner alleged that Jaramillo et al. discloses these features and cited column 6, lines 18-67, of Jaramillo et al. for support. Final Office Action, page 10. Appellant respectfully disagrees.

At column 6, lines 18-67, Jaramillo et al. discloses that when a PCI initiator agent attempts to access a PCI target agent, the PCI target agent issues a bus denial signal to the PCI arbiter so that the PCI arbiter will deny the PCI initiator agent bus access. Nowhere in this section, or elsewhere, does Jaramillo et al. disclose or suggest a switch signal and a select signal, let alone a plurality of slave devices that are configured to select bus mastership using the switch signal and the select signal when the control signals indicate that two or more of the master devices concurrently assert bus mastership, as required by claim 27.

Accordingly, it is respectfully submitted that claim 27 is patentable over Jaramillo et al. and Wang et al., whether taken alone or in any reasonable combination, under 35 U.S.C. § 103. Reversal of the rejection of claim 27 is respectfully requested.

C. Rejection Under 35 U.S.C. § 103(a) Over Jaramillo et al. (U.S. Patent No. 6,598,104) in View of Wang et al. (U.S. Patent Application Publication No. US 2004/0098525) and Nakamura (U.S. Patent No. 6,622,191).

1. Claim 3.

As stated above, the initial burden of establishing a prima facie basis to deny patentability to a claimed invention is always upon the Examiner. In re Oetiker, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In rejecting a claim under 35 U.S.C. § 103, the Examiner must provide a factual basis to support the conclusion of obviousness. In re Warner, 379 F.2d 1011, 154 USPQ

173 (CCPA 1967). Based upon the objective evidence of record, the Examiner is required to make the factual inquiries mandated by Graham v. John Deere Co., 86 S.Ct. 684, 383 U.S. 1, 148 USPQ 459 (1966). The Examiner is also required to explain how and why one having ordinary skill in the art would have been led to modify an applied reference and/or combine applied references to arrive at the claimed invention. Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 5 USPQ2d 1434 (Fed. Cir. 1988).

In establishing motivation, it has been consistently held that the requisite motivation to support the conclusion of obviousness is not an abstract concept, but must stem from the prior art as a whole to impel one having ordinary skill in the art to modify a reference or combine references with a reasonable expectation of successfully achieving some particular realistic objective. See, for example, Interconnect Planning Corp. v. Feil, 227 F.2d 1132, 227 USPQ 543 (Fed. Cir. 1985).

With these principles in mind, Appellant submits that dependent claim 3 is patentable over Jaramillo et al., Wang et al., and Nakamura. Dependent claim 3 recites that the one or more alternate control signals include a bus switch signal that indicates whether a change in control of the bus is to occur and a bus select signal that indicates which of the master devices is to be granted control of the bus. Initially, claim 3 depends from claim 1. The disclosure of Nakamura does not cure the deficiencies in the disclosures of Jaramillo et al. and Wang et al. identified above with regard to claim 1. Claim 3 is, therefore, patentable over Jaramillo et al., Wang et al., and Nakamura, whether taken alone or in any reasonable combination, for at least the reasons given with regard to claim 1.

Further, neither Jaramillo et al., Wang et al., nor Nakamura, whether taken alone or in any

reasonable combination, discloses or suggests the combination of features recited in claim 3. For example, neither Jaramillo et al., Wang et al., nor Nakamura discloses or suggests one or more alternate control signals that include a bus switch signal that indicates whether a change in control of the bus is to occur and a bus select signal that indicates which of the master devices is to be granted control of the bus.

The Examiner alleged that Nakamura discloses these features and cited column 20, lines 17-30, of Nakamura for support. Final Office Action, page 10. Appellant respectfully disagrees.

At column 20, lines 11-30, Nakamura discloses:

> 10. A computer system comprising:
>
> means for performing serial transfer of data needed to transfer a bus cycle between first and second buses via a serial transfer line for connecting said first and second buses;
>
> means for detecting a change in a first interrupt signal on said one of said first and second buses, and, when detecting the change in the first interrupt signal, serially transferring control data indicating a state of the interrupt signal from one of said first and second buses to the other bus via said serial transfer line; and
>
> means for outputting a second interrupt signal on said other bus based on said control data transferred to said other bus from said one of said first and second buses and holding a state of the second interrupt signal output on said other bus until new control data indicating a state of a next interrupt signal arrives.

In this section, Nakamura discloses a first interrupt signal and a second interrupt signal, which the Examiner apparently equates to the bus switch signal and the bus select signal. Nowhere in this section, or elsewhere, however, does Nakamura disclose that the first or second interrupt signal indicates whether a change in control of a bus is to occur or that the first or second interrupt signal indicates which of the master devices is to be granted control of the bus, as would be required by claim 3. The disclosures of Jaramillo et al. and Wang et al. provide nothing to cure these deficiencies in the disclosure of Nakamura.

Accordingly, it is respectfully submitted that claim 3 is patentable over Jaramillo et al., Wang et al., and Nakamura, whether taken alone or in any reasonable combination, under 35 U.S.C. § 103. Reversal of the rejection of claim 3 is respectfully requested.

2. Claim 19.

Dependent claim 19 recites that the one or more alternate control signals include a switch signal that indicates whether a change in mastership is to occur and a select signal that indicates which of the master devices is to be granted mastership. Initially, claim 19 depends from claim 18. The disclosure of Nakamura does not cure the deficiencies in the disclosures of Jaramillo et al. and Wang et al. identified above with regard to claim 18. Claim 19 is, therefore, patentable over Jaramillo et al., Wang et al., and Nakamura, whether taken alone or in any reasonable combination, for at least the reasons given with regard to claim 18.

Further, neither Jaramillo et al., Wang et al., nor Nakamura, whether taken alone or in any reasonable combination, discloses or suggests the combination of features recited in claim 19. For example, neither Jaramillo et al., Wang et al., nor Nakamura discloses or suggests one or more alternate control signals that include a switch signal that indicates whether a change in mastership is to occur and a select signal that indicates which of the master devices is to be granted mastership.

The Examiner alleged that Nakamura discloses these features and cited column 20, lines 17-30, of Nakamura for support. Final Office Action, page 10. Appellant respectfully disagrees.

Column 20, lines 11-30, of Nakamura has been reproduced above. In this section, Nakamura discloses a first interrupt signal and a second interrupt signal, which the Examiner apparently equates to the switch signal and the select signal. Nowhere in this section, or

elsewhere, however, does Nakamura disclose that the first or second interrupt signal indicates whether a change in mastership is to occur or that the first or second interrupt signal indicates which of the master devices is to be granted mastership, as would be required by claim 19. The disclosures of Jaramillo et al. and Wang et al. provide nothing to cure these deficiencies in the disclosure of Nakamura.

Accordingly, it is respectfully submitted that claim 19 is patentable over Jaramillo et al., Wang et al., and Nakamura, whether taken alone or in any reasonable combination, under 35 U.S.C. § 103. Reversal of the rejection of claim 19 is respectfully requested.

3. Claim 24.

Dependent claim 24 recites that the one or more alternate control signals include a bus switch signal that indicates whether a change in bus mastership is to occur and a bus select signal that indicates which of the master devices is to be granted bus mastership. Initially, claim 24 depends from claim 23. The disclosure of Nakamura does not cure the deficiencies in the disclosures of Jaramillo et al. and Wang et al. identified above with regard to claim 23. Claim 24 is, therefore, patentable over Jaramillo et al., Wang et al., and Nakamura, whether taken alone or in any reasonable combination, for at least the reasons given with regard to claim 23.

Further, neither Jaramillo et al., Wang et al., nor Nakamura, whether taken alone or in any reasonable combination, discloses or suggests the combination of features recited in claim 24. For example, neither Jaramillo et al., Wang et al., nor Nakamura discloses or suggests one or more alternate control signals that include a bus switch signal that indicates whether a change in bus mastership is to occur and a bus select signal that indicates which of the master devices is to be granted bus mastership.

The Examiner alleged that Nakamura discloses these features and cited column 20, lines 17-30, of Nakamura for support. Final Office Action, page 10. Appellant respectfully disagrees.

Column 20, lines 11-30, of Nakamura has been reproduced above. In this section, Nakamura discloses a first interrupt signal and a second interrupt signal, which the Examiner apparently equates to the bus switch signal and the bus select signal. Nowhere in this section, or elsewhere, however, does Nakamura disclose that the first or second interrupt signal indicates whether a change in bus mastership is to occur or that the first or second interrupt signal indicates which of the master devices is to be granted bus mastership, as would be required by claim 24. The disclosures of Jaramillo et al. and Wang et al. provide nothing to cure these deficiencies in the disclosure of Nakamura.

Accordingly, it is respectfully submitted that claim 24 is patentable over Jaramillo et al., Wang et al., and Nakamura, whether taken alone or in any reasonable combination, under 35 U.S.C. § 103. Reversal of the rejection of claim 24 is respectfully requested.

D. Rejection Under 35 U.S.C. § 103(a) Over Jaramillo et al. (U.S. Patent No. 6,598,104) in View of Wang et al. (U.S. Patent Application Publication No. US 2004/0098525) and Melo et al. (U.S. Patent No. 5,553,248).

1. Claim 4.

As stated above, the initial burden of establishing a prima facie basis to deny patentability to a claimed invention is always upon the Examiner. In re Oetiker, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In rejecting a claim under 35 U.S.C. § 103, the Examiner must provide a factual basis to support the conclusion of obviousness. In re Warner, 379 F.2d 1011, 154 USPQ 173 (CCPA 1967). Based upon the objective evidence of record, the Examiner is required to

make the factual inquiries mandated by Graham v. John Deere Co., 86 S.Ct. 684, 383 U.S. 1, 148 USPQ 459 (1966). The Examiner is also required to explain how and why one having ordinary skill in the art would have been led to modify an applied reference and/or combine applied references to arrive at the claimed invention. Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 5 USPQ2d 1434 (Fed. Cir. 1988).

In establishing motivation, it has been consistently held that the requisite motivation to support the conclusion of obviousness is not an abstract concept, but must stem from the prior art as a whole to impel one having ordinary skill in the art to modify a reference or combine references with a reasonable expectation of successfully achieving some particular realistic objective. See, for example, Interconnect Planning Corp. v. Feil, 227 F.2d 1132, 227 USPQ 543 (Fed. Cir. 1985).

With these principles in mind, Appellant submits that dependent claim 4 is patentable over Jaramillo et al., Wang et al., and Melo et al. Dependent claim 4 recites bus selection logic configured to determine whether the control signals indicate that none of the master devices asserts control of the bus and maintain a previous grant of control of the bus when none of the master devices asserts control of the bus. Claim 4 depends from claim 1. The disclosure of Melo et al. does not cure the deficiencies in the disclosures of Jaramillo et al. and Wang et al. identified above with regard to claim 1. Claim 4 is, therefore, patentable over Jaramillo et al., Wang et al., and Melo et al., whether taken alone or in any reasonable combination, for at least the reasons given with regard to claim 1.

Accordingly, it is respectfully submitted that claim 4 is patentable over Jaramillo et al., Wang et al., and Melo et al., whether taken alone or in any reasonable combination, under 35 U.S.C. § 103. Reversal of the rejection of claim 4 is respectfully requested.

2. Claim 22.

Dependent claim 22 recites that the selection logic is further configured to select the mastership using the control signals when the control signals indicate that one of the master devices asserts mastership. Claim 22 depends from claim 18. The disclosure of Melo et al. does not cure the deficiencies in the disclosures of Jaramillo et al. and Wang et al. identified above with regard to claim 18. Claim 22 is, therefore, patentable over Jaramillo et al., Wang et al., and Melo et al., whether taken alone or in any reasonable combination, for at least the reasons given with regard to claim 18.

Accordingly, it is respectfully submitted that claim 18 is patentable over Jaramillo et al., Wang et al., and Melo et al., whether taken alone or in any reasonable combination, under 35 U.S.C. § 103. Reversal of the rejection of claim 18 is respectfully requested.

VIII. CONCLUSION

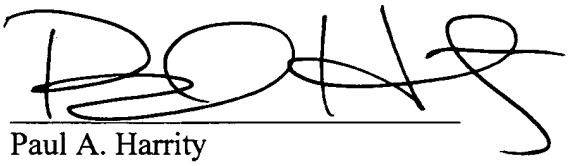
In view of the foregoing arguments, Appellant respectfully solicits the Honorable Board to reverse the Examiner's rejections of claims 1-28 under 35 U.S.C. §§ 102 and 103.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper,

including extension of time fees, to Deposit Account No. 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

HARRITY & SNYDER, L.L.P.



Paul A. Harrity
Reg. No. 39,574

Date: June 30, 2005

11240 Waples Mill Road
Suite 300
Fairfax, Virginia 22030
(571) 432-0800

Customer No. 44987

CLAIM APPENDIX

1. A system for selecting bus mastership in a multi-master system, comprising:

a plurality of master devices configured to generate control signals relating to control of a bus in the multi-master system; and

a plurality of slave devices connected to the master devices via the bus, each of the slave devices being configured to:

receive the control signals from the master devices,

determine whether a conflict in the control signals exists,

generate one or more alternate control signals for selecting bus mastership when a conflict is determined to exist, and

determine which of the master devices obtains control of the bus using the one or more alternate control signals when a conflict is determined to exist.

2. The system of claim 1, wherein each of the slave devices comprises:

bus selection logic configured to determine whether the control signals indicate that two or more of the master devices concurrently assert control of the bus and generate a conflict indication signal when two or more of the master devices concurrently assert control of the bus, and

conflict resolution logic configured to generate the one or more alternate control signals in response to the conflict indication signal.

3. The system of claim 1, wherein the one or more alternate control signals include a

bus switch signal that indicates whether a change in control of the bus is to occur and a bus select signal that indicates which of the master devices is to be granted control of the bus.

4. The system of claim 1, wherein each of the slave devices comprises:

bus selection logic configured to determine whether the control signals indicate that none of the master devices asserts control of the bus and maintain a previous grant of control of the bus when none of the master devices asserts control of the bus.

5. The system of claim 1, wherein each of the slave devices is further configured to determine which of the master devices obtains control of the bus based on the control signals when no conflict is determined to exist.

6. The system of claim 1, wherein the control signals include a present signal that indicates whether a corresponding one of the master devices is operating and a master signal that indicates whether a corresponding one of the master devices asserts control of the bus.

7. The system of claim 1, wherein the control signals include a master signal that indicates whether a corresponding one of the master devices asserts control of the bus.

8. A system for selecting a master in a multi-master system, comprising:

means for outputting first and second control signals relating to mastership in the multi-master system from each of a plurality of masters in the multi-master system;

means for determining whether a conflict for mastership exists based on the first and second control signals;

means for generating a switch signal and a select signal when a conflict is determined to exist; and

means for selecting one of the masters using the switch signal and the select signal.

9. A method for selecting a bus in a multi-bus system, comprising:

generating control signals relating to bus selection in the multi-bus system;

determining whether a conflict for bus selection exists based on the control signals;

generating one or more alternate control signals when a conflict is determined to exist; and

selecting a bus using the one or more alternate control signals.

10. The method of claim 9, wherein the determining includes:

determining whether the control signals indicate that two or more of the buses are to be selected concurrently, and

generating a conflict indication signal when the control signals indicate that two or more of the buses are to be selected concurrently.

11. The method of claim 10, wherein the generating one or more alternate control signals includes:

generating the one or more alternate control signals in response to the conflict indication

signal.

12. The method of claim 9, wherein the one or more alternate control signals include a bus switch signal that indicates whether a change in bus selection is to occur and a bus select signal that indicates which of the buses is to be selected.

13. The method of claim 9, further comprising:

determining whether the control signals indicate that the buses are idle; and

maintaining a previous bus selection when the control signals indicate that the buses are idle.

14. The method of claim 9, further comprising:

selecting a bus using the control signals when no conflict is determined to exist.

15. The method of claim 9, wherein the control signals include a present signal that indicates whether a corresponding bus is operating and a master signal that indicates whether a corresponding bus is to be used.

16. The method of claim 9, wherein the control signals include a master signal that indicates whether a corresponding bus is to be used.

17. A computer-readable medium that stores instructions executable by one or more

processors to perform a method for selecting a master in a multi-master system, comprising:

instructions for outputting a plurality of control signals relating to selection of a master from each of a plurality of masters in the multi-master system;

instructions for determining whether a conflict for selection of a master exists based on the control signals;

instructions for generating a switch control signal and a select control signal when a conflict is determined to exist; and

instructions for selecting one of the masters using the switch control signal and the select control signal.

18. In a multi-master system comprising a plurality of master devices connected to a plurality of slave devices, each of the slave devices comprising:

selection logic configured to determine whether control signals from the master devices indicate that two or more of the master devices concurrently assert mastership within the multi-master system, generate a conflict indication signal when two or more of the master devices concurrently assert mastership, and select mastership using one or more alternate control signals when two or more of the master devices concurrently assert mastership; and

conflict resolution logic configured to generate the one or more alternate control signals to identify mastership in response to the conflict indication signal.

19. The slave device of claim 18, wherein the one or more alternate control signals include a switch signal that indicates whether a change in mastership is to occur and a select

signal that indicates which of the master devices is to be granted mastership.

20. The slave device of claim 18, wherein the control signals include a present signal that indicates whether a corresponding one of the master devices is operating and a master signal that indicates whether a corresponding one of the master devices asserts mastership.

21. The slave device of claim 18, wherein the control signals include a master signal that indicates whether a corresponding one of the master devices asserts mastership.

22. The slave device of claim 18, wherein the selection logic is further configured to select the mastership using the control signals when the control signals indicate that one of the master devices asserts mastership.

23. A method for selecting bus mastership in a multi-master system comprising a plurality of master devices connected to a plurality of slave devices via at least one bus, the method, performed by each of the slave devices, comprising:

determining whether control signals from the master devices indicate that two or more of the master devices concurrently assert bus mastership;

generating one or more alternate control signals to identify which of the master devices obtains bus mastership when two or more of the master devices concurrently assert bus mastership;

determining which of the master devices obtains bus mastership using the one or more

alternate control signals when two or more of the master devices concurrently assert bus mastership; and

determining which of the master devices obtains bus mastership using the control signals when one of the master devices asserts bus mastership.

24. The method of claim 23, wherein the one or more alternate control signals include a bus switch signal that indicates whether a change in bus mastership is to occur and a bus select signal that indicates which of the master devices is to be granted bus mastership.

25. The method of claim 23, wherein the control signals include a present signal that indicates whether a corresponding one of the master devices is operating and a master signal that indicates whether a corresponding one of the master devices asserts bus mastership.

26. The method of claim 23, wherein the control signals include a master signal that indicates whether a corresponding one of the master devices asserts bus mastership.

27. A multi-master system, comprising:

a plurality of master devices configured to generate control signals relating to bus mastership;

conflict resolution logic configured to receive the control signals from the master devices, determine whether the control signals indicate that two or more of the master devices concurrently assert bus mastership, and generate a switch signal and a select signal when it is

determined that two or more of the master devices concurrently assert bus mastership; and

a plurality of slave devices configured to select bus mastership using the switch signal and the select signal when the control signals indicate that two or more of the master devices concurrently assert bus mastership.

28. A multi-bus system, comprising:

a plurality of buses;

a plurality of master devices corresponding to the buses, each of the master devices controlling a corresponding one of the buses, the master devices generating control signals that indicate which of the buses is an active bus; and

a plurality of slave devices connected to each of the buses and configured to receive the control signals, determine whether the control signals indicate that two or more of the buses are declared active buses, generate alternate control signals when the control signals indicate that two or more of the buses are declared active buses, and select one of the buses as the active bus using the alternate control signals.

Patent
Attorney's Docket No. 0023-0003

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)	
	)	
Ross Suydam HEITKAMP	)	Group Art Unit: 2112
	)	
Application No.: 09/749,585	)	Examiner: K. Huynh
	)	
Filed: December 28, 2000	)	
	)	
For: SYSTEMS AND METHODS FOR RELIABLY SELECTING BUS MASTERSHIP IN A FAULT TOLERANT MANNER	)	

TRANSMITTAL FOR APPEAL BRIEF

U.S. Patent and Trademark Office
Customer Service Window, Mail Stop Appeal Brief-Patents
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Sir:

Transmitted herewith is an Appeal Brief in support of the Notice of Appeal filed May 4, 2005.

Enclosed is a check for ☐ $250.00 ☒ $500.00 to cover the Government fee.

The Commissioner is hereby authorized to charge any other appropriate fees that may be required by this paper that are not accounted for above, and to credit any overpayment, to Deposit Account No. 50-1070.

Respectfully submitted,

HARRITY & SNYDER, L.L.P.

By: _____
Paul A. Harrity
Reg. No. 39,574

11240 Waples Mill Road
Suite 300
Fairfax, Virginia 22030
(571) 432-0800
CUSTOMER NUMBER: 44987
Date: June 30, 2005